

METHOD AND APPARATUS FOR REDUCING CAPACITIVE
COUPLING BETWEEN LINES IN AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

5 An integrated circuit (78) includes a memory circuit
(10, 110, 210, 310, 410) having a group of bitlines (21-28,
121-128, 221-228, 321-328, 421-428), and having an array of
memory cells (11-18) which are each electrically coupled to
two bitlines of the group. Each bitline has alternating
first (61, 63, 65) and second (62, 64, 66) portions that
are respectively located in metalization layers disposed on
opposite sides of an insulating layer (84). The first and
10 second portions are electrically coupled by vias (51-54,
334, 437) which extend through the insulating layer. Along
the length of each bitline, each first and second portion
thereof is disposed in a metalization layer opposite from
the metalization layer containing the adjacent portion of
15 each adjacent bitline.